CLAIMS

1. A data processing apparatus operable to map input symbols to be communicated onto a predetermined number of carrier signals of an Orthogonal Frequency Division Multiplexed (OFDM) symbol, the data processing apparatus comprising

an interleaver memory operable to read-in the predetermined number of data symbols for mapping onto the OFDM carrier signals, and to read-out the data symbols for the OFDM carriers to effect the mapping, the read-out being in a different order than the read-in, the order being determined from a set of addresses, with the effect that the data symbols are interleaved on the carrier signals,

an address generator operable to generate the set of addresses, an address being generated for each of the input symbols to indicate one of the carrier signals onto which the data symbol is to be mapped, the address generator comprising

a linear feedback shift register including a predetermined number of register stages and being operable to generate a pseudo-random bit sequence in accordance with a generator polynomial,

a permutation circuit operable to receive the content of the shift register stages and to permute the bits present in the register stages in accordance with a permutation order to form an address of one of the OFDM carriers, and

a control unit operable in combination with an address check circuit to re-generate an address when a generated address exceeds the predetermined number of carriers, characterised in that

the predetermined number of OFDM carrier signals is substantially four thousand,

the linear feedback shift register has eleven register stages with a generator polynomial for the linear feedback shift register of $R_i'[10] = R_{i-1}'[0] \oplus R_{i-1}'[2]$, and the permutation order forms an eleven bit address $R_i[n]$ for the i-th data symbol from the bit present in the n-th register stage $R_i'[n]$ in accordance with the table:

$R_i'[n]$ for n =	10	9	8	7	6	5	4	3	2	1	0
$R_i[n]$ for n =	7	10	5	8	1	2	4	9	0	3	6

2. A data processing apparatus as claimed in Claim 1, wherein the predetermined number of carrier signals is three thousand and twenty four.

3. A data processing apparatus as claimed in Claim 1, wherein the interleaver memory is operable to effect the mapping of the input data symbols onto the carrier signals for even OFDM symbols by reading in the data symbols according to the set of addresses generated by the address generator and reading out in a sequential order, and for odd OFDM symbols by reading in the symbols into the memory in a sequential order and reading out the data symbols from the memory in accordance with the set of addresses generated by the address generator.

4. A transmitter for transmitting data using Orthogonal Frequency Division Multiplexing (OFDM), the transmitter including a data processing apparatus according to any preceding Claim.

5. A transmitter as claimed in Claim 4, wherein the transmitter is operable to transmit data in accordance with the Digital Video Broadcasting-Terrestrial or Digital Video Broadcasting-Handheld standard.

6. A data processing apparatus operable to de-map symbols received from a predetermined number of carrier signals of an Orthogonal Frequency Division Multiplexed (OFDM) symbol into an output symbol stream, the data processing apparatus comprising

a de-interleaver memory operable to read-in the predetermined number of data symbols from the OFDM carrier signals, and to read-out the data symbols into the output symbol stream to effect the de-mapping, the read-out being in a different order than the read-in, the order being determined from a set of addresses, with the effect that the data symbols are de-interleaved from the OFDM carrier signals,

an address generator operable to generate the set of addresses, an address being generated for each of the received data symbols to indicate the OFDM carrier signal from which the received data symbol is to be de-mapped into the output symbol stream, the address generator comprising

a linear feedback shift register including a predetermined number of register stages and being operable to generate a pseudo-random bit sequence in accordance with a generator polynomial,

a permutation circuit operable to receive the content of the shift register stages and to permute the bits present in the register stages in accordance with a permutation order to form an address of one of the OFDM carriers, and

a control unit operable in combination with an address check circuit to re-generate an address when a generated address exceeds the predetermined number of carriers, characterised in that

the predetermined number of OFDM carrier signals is substantially four thousand,

the linear feedback shift register has eleven register stages with a generator polynomial for the linear feedback shift register of $R_i'[10] = R_{i-1}'[0] \oplus R_{i-1}'[2]$, and the permutation order forms an eleven bit address $R_i[n]$ for the i-th data symbol from the bit present in the n-th register stage $R_i'[n]$ in accordance with the table:

$R_i'[n]$ for n =	10	9	8	7	6	5	4	3	2	1	0
$R_i[n]$ for n =	7	10	5	8	1	2	4	9	0	3	6

7. A data processing apparatus as claimed in Claim 6, wherein the predetermined number of carrier signals is three thousand and twenty four.

8. A data processing apparatus as claimed in Claim 6, wherein the de-interleaver memory is arranged to effect the de-mapping of the received data symbols from the carrier signals onto the output data stream for even OFDM symbols by reading in the data symbols according to a sequential order and reading out the data symbols from memory according to the set of addresses generated by the address generator, and for odd OFDM symbols by reading in the symbols into the memory in accordance with the set of addresses generated by the address generator and reading out the data symbols from the memory in accordance with a sequential order.

9. A receiver for receiving data from Orthogonal Frequency Division Multiplexing (OFDM) modulated signal, the receiver including a data processing apparatus operable to de-map symbols received from a predetermined number of carrier signals of an Orthogonal Frequency Division Multiplexed (OFDM) symbol into an output symbol stream, the data processing apparatus comprising

a de-interleaver memory operable to read-in the predetermined number of data symbols from the OFDM carrier signals, and to read-out the data symbols into the output symbol stream to effect the de-mapping, the read-out being in a different order than the read-in, the order being determined from a set of addresses, with the effect that the data symbols are de-interleaved from the OFDM carrier signals,

an address generator operable to generate the set of addresses, an address being generated for each of the received data symbols to indicate the OFDM carrier signal from which the received data symbol is to be de-mapped into the output symbol stream, the address generator comprising

a linear feedback shift register including a predetermined number of register stages and being operable to generate a pseudo-random bit sequence in accordance with a generator polynomial,

a permutation circuit operable to receive the content of the shift register stages and to permute the bits present in the register stages in accordance with a permutation order to form an address of one of the OFDM carriers, and

a control unit operable in combination with an address check circuit to re-generate an address when a generated address exceeds the predetermined number of carriers, characterised in that

the predetermined number of OFDM carrier signals is substantially four thousand,

the linear feedback shift register has eleven register stages with a generator polynomial for the linear feedback shift register of $R_i'[10] = R_{i-1}'[0] \oplus R_{i-1}'[2]$, and the permutation order forms an eleven bit address $R_i[n]$ for the i-th data symbol from the bit present in the n-th register stage $R_i'[n]$ in accordance with the table:

$R_i'[n]$ for n =	10	9	8	7	6	5	4	3	2	1	0
$R_i[n]$ for n =	7	10	5	8	1	2	4	9	0	3	6

10. A receiver as claimed in Claim 9, wherein the receiver is operable to receive data which has been modulated in accordance with the Digital Video Broadcasting-Terrestrial or Handheld standard.

11. A method of mapping input symbols to be communicated onto a predetermined number of carrier signals of an Orthogonal Frequency Division Multiplexed (OFDM) symbol, the method comprising

reading-in the predetermined number of data symbols for mapping onto the OFDM carrier signals,

reading-out the data symbols for the OFDM carriers to effect the mapping, the read-out being in a different order than the read-in, the order being determined from a set of addresses, with the effect that the data symbols are interleaved on the carrier signals,

generating the set of addresses, an address being generated for each of the input symbols to indicate one of the carrier signals onto which the data symbol is to be mapped, the generating the set of addresses comprising

using a linear feedback shift register including a predetermined number of register stages to generate a pseudo-random bit sequence in accordance with a generator polynomial,

using a permutation circuit operable to receive the content of the shift register stages to permute the bits present in the register stages in accordance with a permutation order to form an address of one of the of OFDM carriers, and

re-generating an address when a generated address exceeds the predetermined number of carriers, characterised in that

the predetermined number of OFDM carrier signals is substantially four thousand,

the linear feedback shift register has eleven register stages with a generator polynomial for the linear feedback shift register of $R_i'[10] = R_{i-1}'[0] \oplus R_{i-1}'[2]$, and the

permutation order forms an eleven bit address $R_i[n]$ for the i-th data symbol from the bit present in the n-th register stage $R_i'[n]$ in accordance with the table:

$R_i'[n]$ for n =	10	9	8	7	6	5	4	3	2	1	0
$R_i[n]$ for n =	7	10	5	8	1	2	4	9	0	3	6

12. A method of de-mapping symbols received from a predetermined number of carrier signals of an Orthogonal Frequency Division Multiplexed (OFDM) symbol into an output symbol stream, the method comprising

reading-in the predetermined number of data symbols from the OFDM carrier signals,

reading-out the data symbols into the output symbol stream to effect the de-mapping, the read-out being in a different order than the read-in, the order being determined from a set of addresses, with the effect that the data symbols are de-interleaved from the OFDM carrier signals,

generating the set of addresses, an address being generated for each of the received symbols to indicate the OFDM carrier signal from which the received data symbol is to be de-mapped into the output symbol stream, the generating the set of addresses comprising

using a linear feedback shift register including a predetermined number of register stages to generate a pseudo-random bit sequence in accordance with a generator polynomial,

using a permutation circuit to receive the content of the shift register stages and to permute the bits present in the register stages in accordance with a permutation order to form an address of one of the OFDM carriers, and

re-generating an address when a generated address exceeds the predetermined number of carriers, characterised in that

the predetermined number of OFDM carrier signals is substantially four thousand,

the linear feedback shift register has eleven register stages with a generator polynomial for the linear feedback shift register of $R_i'[10] = R_{i-1}'[0] \oplus R_{i-1}'[2]$, and the

permutation order forms an eleven bit address $R_i[n]$ for the i-th data symbol from the bit present in the n-th register stage $R_i'[n]$ in accordance with the table:

$R_i'[n]$ for n =	10	9	8	7	6	5	4	3	2	1	0
$R_i[n]$ for n =	7	10	5	8	1	2	4	9	0	3	6

13. An address generator for use with transmission or reception of data symbols interleaved onto substantially four thousand carriers of an Orthogonal Frequency Division Multiplexed symbol, the address generator being operable to generate a set of addresses, each address being generated for each of the data symbols to indicate one of the carrier signals onto which the data symbol is to be mapped or de-mapped, the address generator comprising

a linear feedback shift register including a predetermined number of register stages and being operable to generate a pseudo-random bit sequence in accordance with a generator polynomial,

a permutation circuit operable to receive the content of the shift register stages and to permute the bits present in the register stages in accordance with a permutation order to form an address of one of the OFDM carriers, and

a control unit operable in combination with an address check circuit to re-generate an address when a generated address exceeds the predetermined number of carriers, characterised in that

the linear feedback shift register has eleven register stages with a generator polynomial for the linear feedback shift register of $R_i'[10] = R_{i-1}'[0] \oplus R_{i-1}'[2]$, and the permutation order forms an eleven bit address $R_i[n]$ for the i-th data symbol from the bit present in the n-th register stage $R_i'[n]$ in accordance with the table:

$R_i'[n]$ for n =	10	9	8	7	6	5	4	3	2	1	0
$R_i[n]$ for n =	7	10	5	8	1	2	4	9	0	3	6

14. A data processing apparatus for mapping input symbols to be communicated onto a predetermined number of carrier signals of an Orthogonal Frequency Division Multiplexed (OFDM) symbol, the apparatus comprising

means for reading-in the predetermined number of data symbols for mapping onto the OFDM carrier signals,

means for reading-out the data symbols for the OFDM carriers to effect the mapping, the read-out being in a different order than the read-in, the order being determined from a set of addresses, with the effect that the data symbols are interleaved on the carrier signals,

means for generating the set of addresses, an address being generated for each of the input symbols to indicate one of the carrier signals onto which the data symbol is to be mapped, the means for generating the set of addresses comprising

means for using a linear feedback shift register including a predetermined number of register stages to generate a pseudo-random bit sequence in accordance with a generator polynomial,

means for using a permutation circuit operable to receive the content of the shift register stages to permute the bits present in the register stages in accordance with a permutation order to form an address of one of the of OFDM carriers, and

means for re-generating an address when a generated address exceeds the predetermined number of carriers, characterised in that

the predetermined number of OFDM carrier signals is substantially four thousand,

the linear feedback shift register has eleven register stages with a generator polynomial for the linear feedback shift register of $R_i'[10] = R_{i-1}'[0] \oplus R_{i-1}'[2]$, and the permutation order forms an eleven bit address $R_i[n]$ for the i-th data symbol from the bit present in the n-th register stage $R_i'[n]$ in accordance with the table:

$R_i'[n]$ for n =	10	9	8	7	6	5	4	3	2	1	0
$R_i[n]$ for n =	7	10	5	8	1	2	4	9	0	3	6

15. A data processing apparatus for de-mapping symbols received from a predetermined number of carrier signals of an Orthogonal Frequency Division Multiplexed (OFDM) symbol into an output symbol stream, the apparatus comprising

means for reading-in the predetermined number of data symbols from the OFDM carrier signals,

means for reading-out the data symbols into the output symbol stream to effect the de-mapping, the read-out being in a different order than the read-in, the order being determined from a set of addresses, with the effect that the data symbols are de-interleaved from the OFDM carrier signals,

means for generating the set of addresses, an address being generated for each of the received symbols to indicate the OFDM carrier signal from which the received data symbol is to be de-mapped into the output symbol stream, the means for generating the set of addresses comprising

means for using a linear feedback shift register including a predetermined number of register stages to generate a pseudo-random bit sequence in accordance with a generator polynomial,

means for using a permutation circuit to receive the content of the shift register stages and to permute the bits present in the register stages in accordance with a permutation order to form an address of one of the OFDM carriers, and

means for re-generating an address when a generated address exceeds the predetermined number of carriers, characterised in that

the predetermined number of OFDM carrier signals is substantially four thousand,

the linear feedback shift register has eleven register stages with a generator polynomial for the linear feedback shift register of $R_i'[10] = R_{i-1}'[0] \oplus R_{i-1}'[2]$, and the permutation order forms an eleven bit address $R_i[n]$ for the i-th data symbol from the bit present in the n-th register stage $R_i'[n]$ in accordance with the table:

$R_i'[n]$ for n =	10	9	8	7	6	5	4	3	2	1	0
$R_i[n]$ for n =	7	10	5	8	1	2	4	9	0	3	6